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Cisco C9610R Series Smart Switches:
Feature & Performance Validation Assessment

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1.0 Executive Summary

As enterprises continue to grow, they require high-capacity campus cores that deliver scale, resiliency, and operational clarity. Modular switching platforms are central to this architecture, providing the high port density, exceptional bandwidth, and robustness necessary for a future-proof workplace.

Cisco engaged Miercom to evaluate the Cisco C9610R Series Smart Switches – the next generation modular platform as the campus core for high-density deployments. Built upon the Cisco Silicon One architecture, the C9000 series smart switches provide a unified, programmable silicon foundation that ensures industry-leading performance, high port density, and superior energy efficiency. These switches are also engineered for AI readiness, featuring the high-speed connectivity, low latency, and intelligent observability needed to power modern AI-driven enterprise applications and workloads.

The Cisco C9000 Series Smart Switches deliver Full Stack Post-Quantum Cryptography (PQC), providing an end-to-end quantum security architecture from Secure Boot to Secure Transport. The Cisco C9000 Smart Switches feature an integrated Trust Anchor Module (TAm) within an FPGA chip, establishing a hardware-anchored chain of trust enhanced by Post-Quantum Cryptography (PQC). The TAm securely stores PQC keys, which are used to verify PQC-signed Bootloader and IOS XE images, ensuring only trusted software is loaded during bootup. Additionally, the bus interfaces between the TAm and CPU are protected with PQC to prevent confidential information from leaking. Secure Boot ensures the switch is protected from the moment it powers on. For Secure Transport, Cisco IOS XE supports PQC algorithms for protocols such as MACsec, IPsec, SSH, and TLS, ensuring protection against future quantum-enabled attacks. Full Stack PQC ensures robust, end-to-end quantum safety, making the Cisco C9000 Smart Switches uniquely prepared for the evolving cybersecurity landscape.

A standout capability of the C9000 Smart Switches is the new HCAM (Algorithmic Hash-based TCAM). By combining the strengths of TCAM and SRAM, HCAM delivers high-scale ACL and NetFlow performance. This innovative approach offers faster lookups with lower power and heat consumption compared to traditional TCAM, making it a more cost-effective solution for scaling. Beyond efficiency, HCAM serves as a critical engine for full-stack observability. It provides the granular visibility into traffic patterns and telemetry data required to optimize network health and application performance. Simultaneously, its high-scale capacity for Access Control Lists (ACLs) strengthens the overall security posture, enabling robust, hardware-accelerated policy enforcement and micro-segmentation to protect against evolving threats without sacrificing throughput.

Our test program, executed with Spirent Test Center, models real production conditions and controller workflows to validate forwarding behavior, control-plane scale, and service continuity. The scope covers Layer-2 and Layer-3 forwarding with fixed and IMIX traffic profiles; latency characterization; table scale for MAC addresses and routing entries; high-availability mechanisms (SSO, NSF) and failover continuity; QoS classification, shaping, and queue behavior under stress; and observability via telemetry and automation interfaces. The aim is to confirm architecture fit and datasheet claims for large enterprise campuses and to surface deployment guidance on slot, fabric, and uplink choices.

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Key Findings

- **Line-rate with no loss** across all frame sizes and IMIX. Aggregate throughput remained 100% with zero frame loss from 324 to 9216 bytes; IMIX also achieved 100% with no loss.
- **No small-packet cliff or jumbo penalty**. The latency curve is broadly flat with a modest dip around 4096 bytes; consistency holds through jumbo frames.
- **Observed FIB capacity matched** or exceeded limits. 2,000,037 vs. 2,000,000 and 1,000,035 IPv6 vs. 1,000,000—confirming the switch can carry its indented dual-stack route tables without capacity risk.
- **Hardware-rooted secure boot process**. A Trust Anchor Module (TAM) establishes a chain of trust that validates the bootloader and IOS XE software images before execution, protecting system integrity at startup.
- **Software image integrity** is protected through digital signing. Signed image verification prevents unauthorized or modified software from loading on the platform and provides a foundation for future quantum-resistant signing methods.
- **Post-Quantum Cryptography support** is architectural and forward-looking. The platform aligns with emerging PQC standards while current implementations continue to rely on established cryptographic algorithms for secure boot and image validation.
- **High Availability with Minimal Traffic Impact:** SSO, NSF, and ISSU testing showed forwarding continuity during software upgrades. Traffic disruption was sub-seconds and limited to brief, expected convergence windows, with no full system reloads or manual recovery required.

Miercom observed the performance of the Cisco C9610R Series Smart Switch and awards the ***Miercom Performance Verified*** certification in recognition of its proven performance demonstrating sustained line-rate throughput with zero frame loss across all packet sizes and IMIX, while maintaining consistently low and predictable microsecond-level latency. Forwarding scale met or exceeded published dual-stack FIB capacities without degradation, and performance remained stable across small and jumbo frames. Combined with a hardware-rooted secure boot architecture, forward-looking cryptographic design, and native application hosting, the platform demonstrations a balanced combination of performance, scale and integration security worthy of recognition.

Robert Smithers

CEO, Miercom

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2.0 Products Tested

The Cisco C9610 Supervisor Engine 3/3XL is based on Cisco Silicon One E100/K100 and delivers up to 51.2 Tbps per chassis (6.4 Tbps per slot) with packet processing up to 15.6 Bpps, and scale to 2M IPv4 routes (model-dependent).

2.1 Cisco C9610 Series Smart Switches (C9610R)

The Cisco C9610R is a 10-slot modular chassis that also comes with two new native line cards:

1. C9610-LC-32CD (32x 100G or 24x 100G + 2x 400G)
2. C9610-LC-40YL4CD

The Cisco C9610R also supports the current Catalyst 9600 Series line cards.

The Cisco C9610R Chassis scales up to 256×100G, depending on line-card configuration.

Supported interface families across the series (line-card dependent):

- 400/200/100 G QSFP-DD (200 G QSFP56 is hardware capable)
- 100/40 G QSFP28
- 50/25/10/1 G SFP56/SFP28/SFP+/SFP
- 10/1 G RJ-45 copper ports

Cisco C9610R 10-slot chassis – 2 supervisor slots + 8 line-card slots; supports Catalyst 9600 Series line cards; up to 51.2 Tbps switching capacity (6.4 Tbps/slot) with system densities up to 256×100G or 16×400G; StackWise Virtual supported.

Cisco C9610 Supervisor Engine 3 / 3XL

C9610-SUP-3 and C9610-SUP-3XL use Cisco Silicon One E100/K100 and provide 6.4 Tbps per slot (up to 51.2 Tbps per chassis), with high-availability features StackWise-Virtual/SSO/ISSU and support for 400G QSFP-DD.

C9610-SUP-3: *Cisco C9610 Supervisor Engine 3 – 4× Silicone One E100 + Q200L;up to 1M IPv4 / 500K IPv6 routes; 256MB QoS buffers; 6.4 Tbps/slot (51.2 Tbps system).*

C9610-SUP-3XL: *Cisco C9610 Supervisor Engine 3XL – 4× Silicone One K100 + Q200L up to 2M IPv4 / 1M IPv6 routes; 256MB + 8GB HBM2E QoS buffers; 6.4 Tbps/slot (51.2 Tbps system).*

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3.0 How We Did It

Business environments were simulated through real-world traffic scenarios for an accurate assessment of product performance. We evaluated the Cisco C9610R with a Spirent Test Center generating traffic from bidirectional test ports, one for each corresponding port on the Device Under Test (DUT).

Traffic consisted of the following packet sizes:

- 64, 128, 256, 400, 512, 1024, 1280, 1518, 2048, 4096, 9198, 9216, IMIX bytes

IMIX traffic breakdown

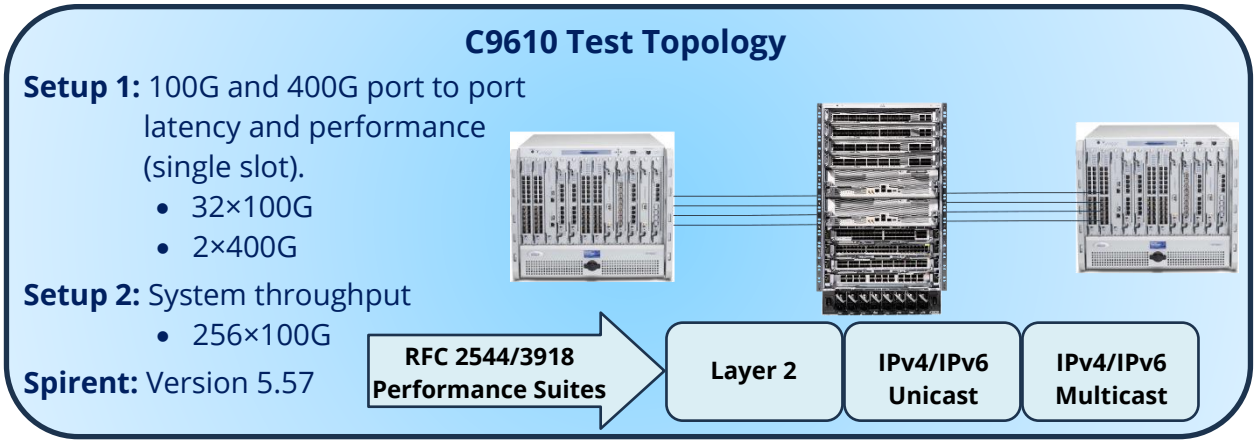
IMIX: IPv4 and IPv6			
IP Total Length	Default Ethernet	Weight	Percentage
64	82	5867	59%
78	96	200	2%
576	594	2366	24%
1500	1518	1567	16%

RFC 2544/3918 Performance Test Coverage:

Layer 2**,** Layer 3 IPv4/IPv6 Unicast, IPv4/IPv6 Multicast

Test Environment:

Cisco IOS-XE Software: 17.18.01
Spirent Test Center: 5.57



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4.0 Cisco C9610R Series Smart Switches

4.1 Cisco C9610R Full Chassis Capacity Test

Performance was tested using RFC 2544 for throughput and latency measurements and RFC 3918 for multicast testing. All ports are open and use Layer 2 and Layer 3 traffic.

Using a fully populated C9610R chassis with C9610-LC-32CD line cards (32x 100G or 24 × 100G + 2 × 400G per card), the switch was exercised for full load capacity across the system. The system throughput “snake” view targets 256 × 100G, and the single-slot port-to-port view includes 32 × 100G for latency and performance. The following frame sizes were generated: 64, 128, 256, 512, 1024, 1280, 1518, 2048, 4096, 9198, 9216, IMIX.

Load levels:

All Stream Blocks: 10%, 25%, 100%

This test determined the maximum rate at which the DUT received and forwarded traffic across all ports without frame loss. Frames were generated at increasing rates through the DUT; latency was recorded in microseconds (µs) as the difference in timestamps between packets sent and received by Spirent TestCenter.

The DUT was configured, in accordance with RFC 2544 and RFC 3918, to endure a stress test of the following load distributions traversing local and other line cards (traffic forced across the fabric).

- Layer 3 – IPv4, IPv6
- Layer 2

The Spirent TestCenter was configured to forward and receive traffic to and from each directly connected port on the switch. Frames were initially sent at the theoretically rated throughput of the port, and if successfully processed by the DUT, the switch was said to have achieved wire speed or full line rate. Throughput was measured as the highest percentage of theoretical line rate successfully achieved.

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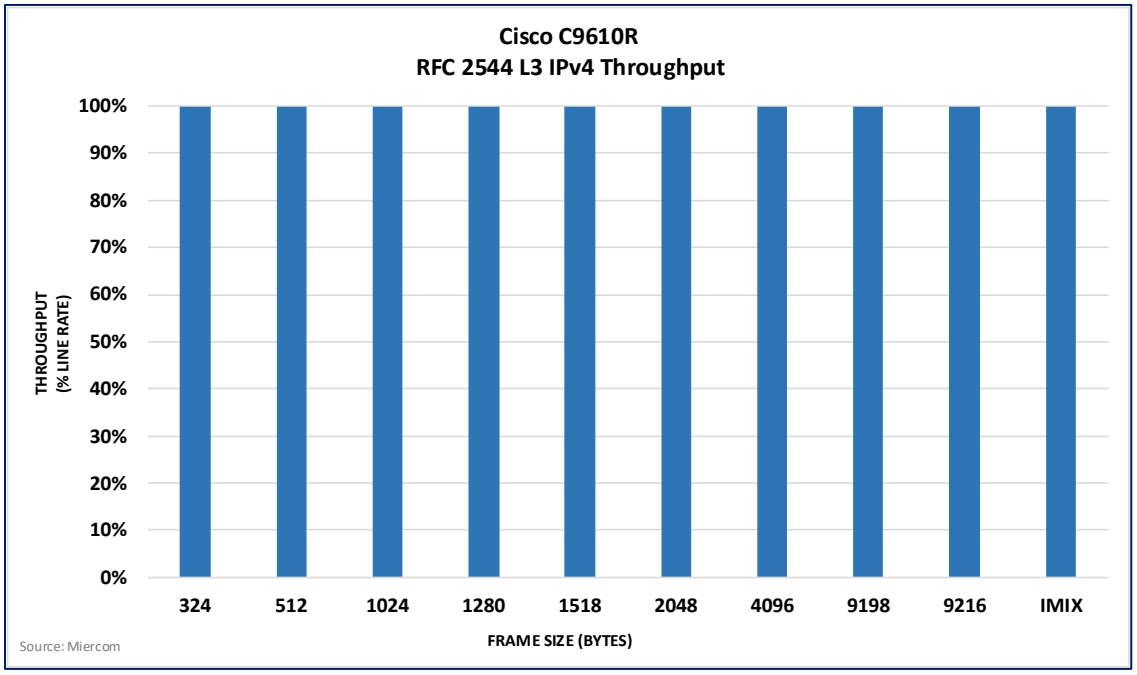
4.1.1 Cisco C9610R L3 IPv4 Unicast

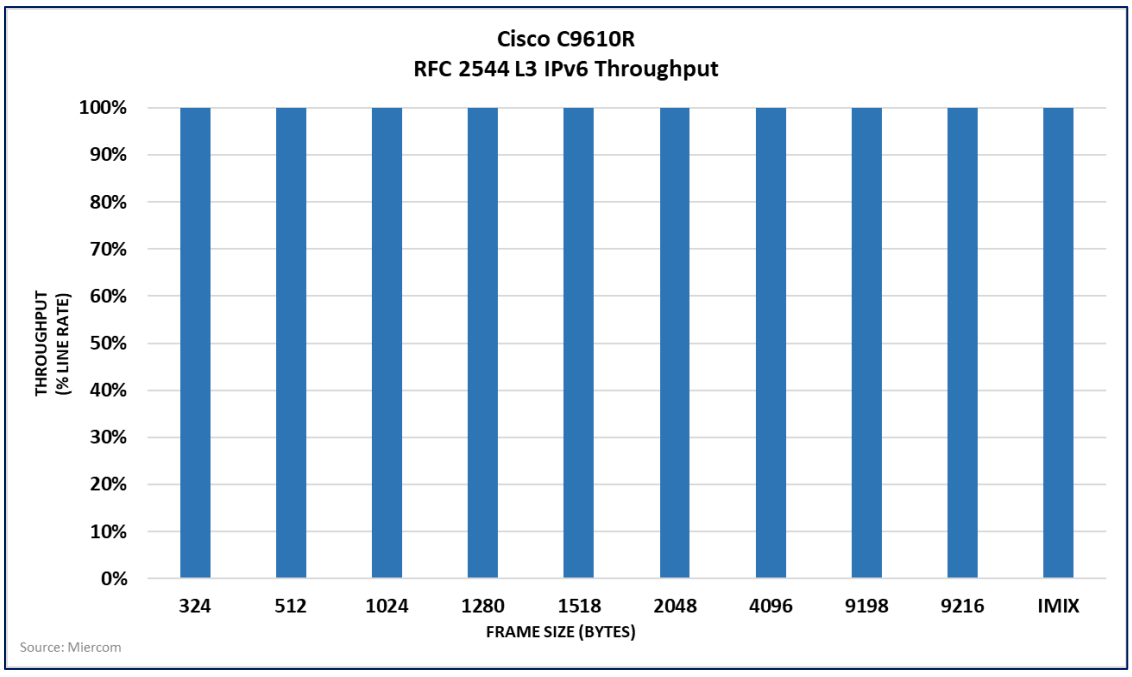
The Cisco C9610R delivered full line rate for all frame sizes and IMIX with all 100G ports loaded.



Cisco C9610R full-chassis capacity with eight C9610-LC-32CD line cards in a 100G snake topology, RFC 2544 L3 IPv4 latency by frame size: minimum ~49–64 µs, average ~72–86 µs, maximum up to ~87 µs; IMIX measured 52.7 µs minimum, 83.2 µs average, 87.1 µs maximum.

4.1.2 Cisco C9610R L3 IPv6 Unicast

The Cisco C9610R delivered full line-rate for all frame sizes and IMIX with all 100G ports loaded.



Cisco C9610R full-chassis capacity with eight C9610-LC-32CD line cards in a 100G snake topology, RFC 2544 L3 IPv4 throughput: 100%-line rate at every tested frame size, including IMIX.

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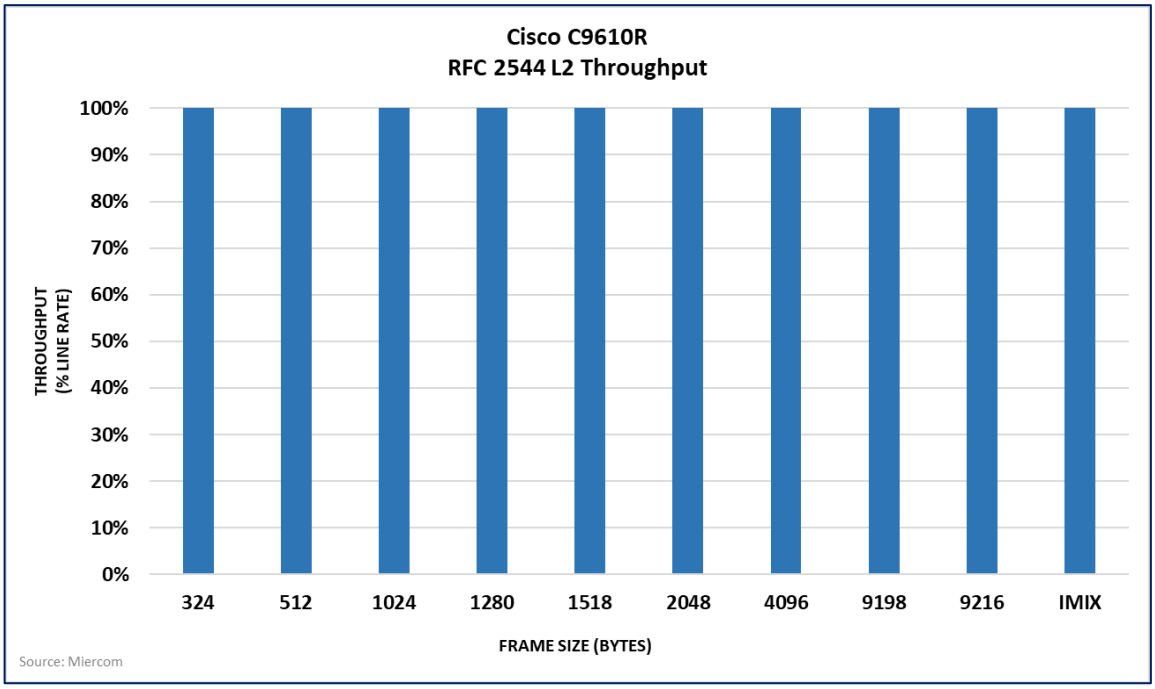
4.1.3 Cisco C9610R L2

In Layer 2 testing, the Cisco C9610R delivered full line-rate performance at all tested frame sizes from 324 to 9216 with the chassis fully populated with eight C9610-LC-32CD 100G line cards in a 256×100G port to port configuration, and it sustained line rate on IMIX.

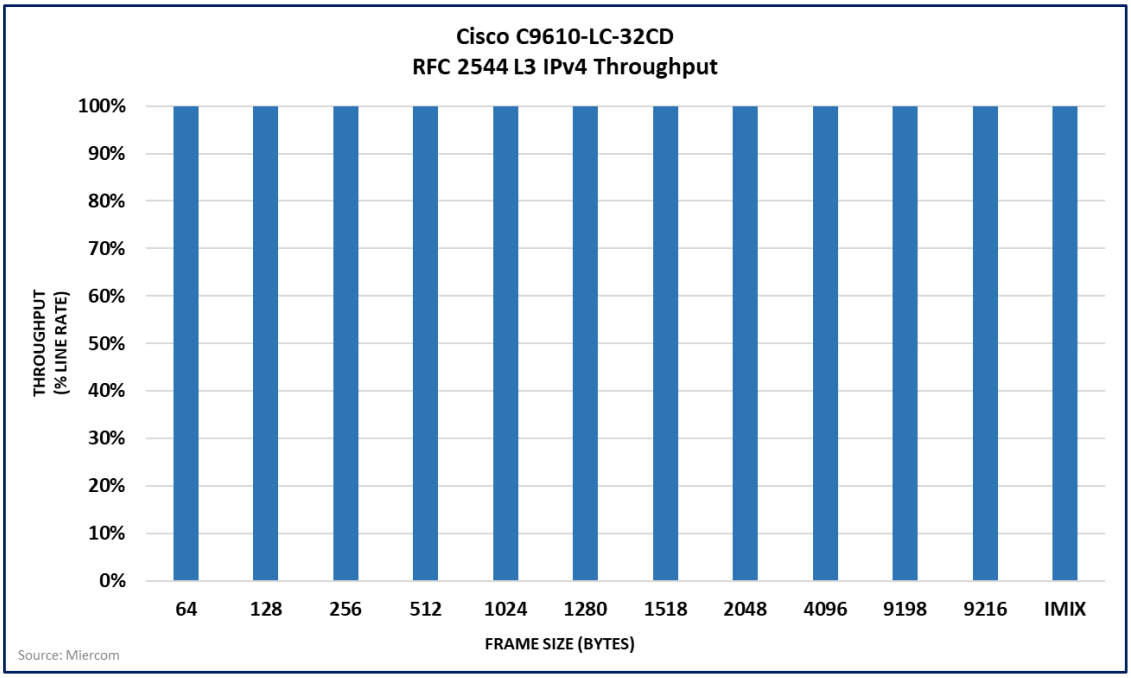


Cisco C9610R chassis populated with eight C9610-LC-32CD 100G line cards, 256×100G snake configuration. RFC 2544 Layer 2 throughput achieved line rate at every tested frame size and on IMIX.

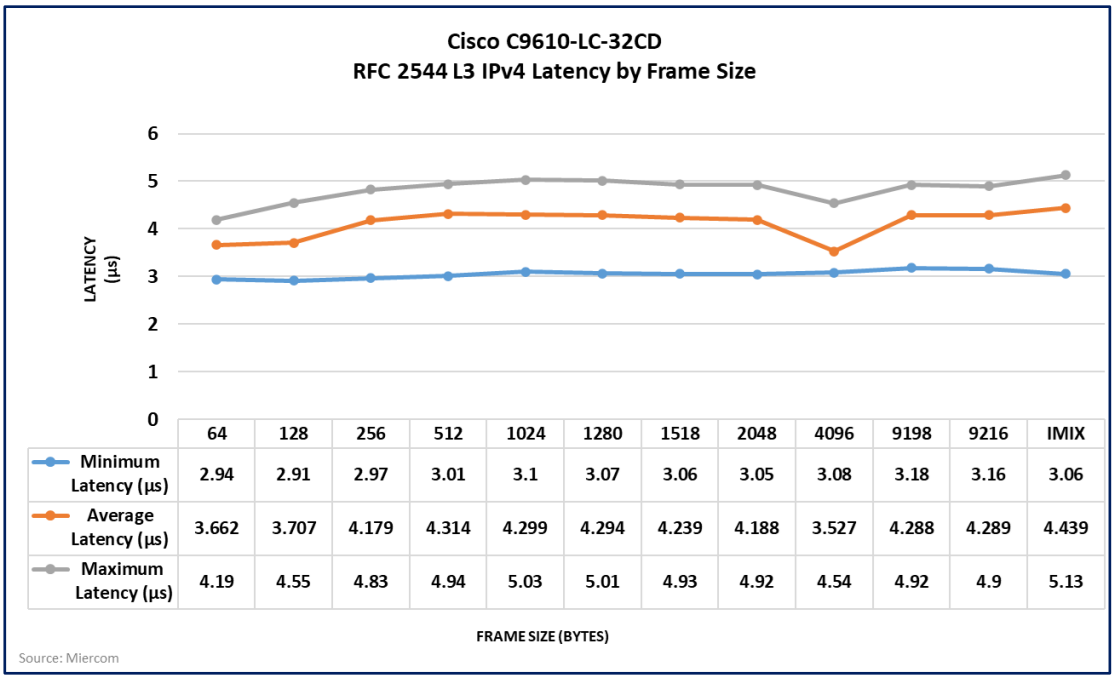
4.2 Cisco C9610R Performance and Latency

4.2.1 Cisco C9610-LC-32CD L3 IPv4 100G Unicast

The Cisco C9610-LC-32CD delivered full line-rate performance for all frame sizes with all 100G ports loaded. Frame loss was zero throughout.



Cisco C9610-LC-32CD sustained full line-rate across all frame sizes with all test ports active. Throughput remained at 100% with zero frame loss from 64 to 9216 bytes IMIX also achieved 100% with no loss.



	64	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	2.94	2.91	2.97	3.01	3.1	3.07	3.06	3.05	3.08	3.18	3.16	3.06
Average Latency (µs)	3.662	3.707	4.179	4.314	4.299	4.294	4.239	4.188	3.527	4.288	4.289	4.439
Maximum Latency (µs)	4.19	4.55	4.83	4.94	5.03	5.01	4.93	4.92	4.54	4.92	4.9	5.13

Cisco C9610-LC-32CD maintained lossless, line-rate across all frame sizes and IMIX during RFC 2544 Layer-3 IPv4 testing. Latency stayed in the low- µs range across fixed sizes with a dip in average near 4096 bytes.

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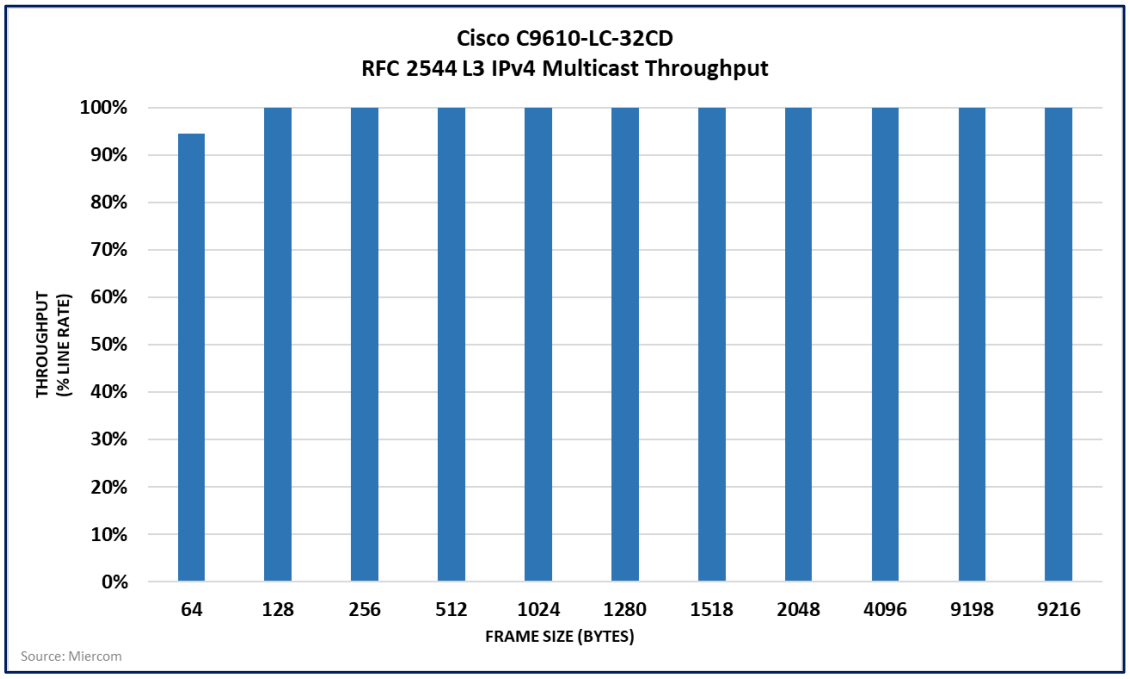
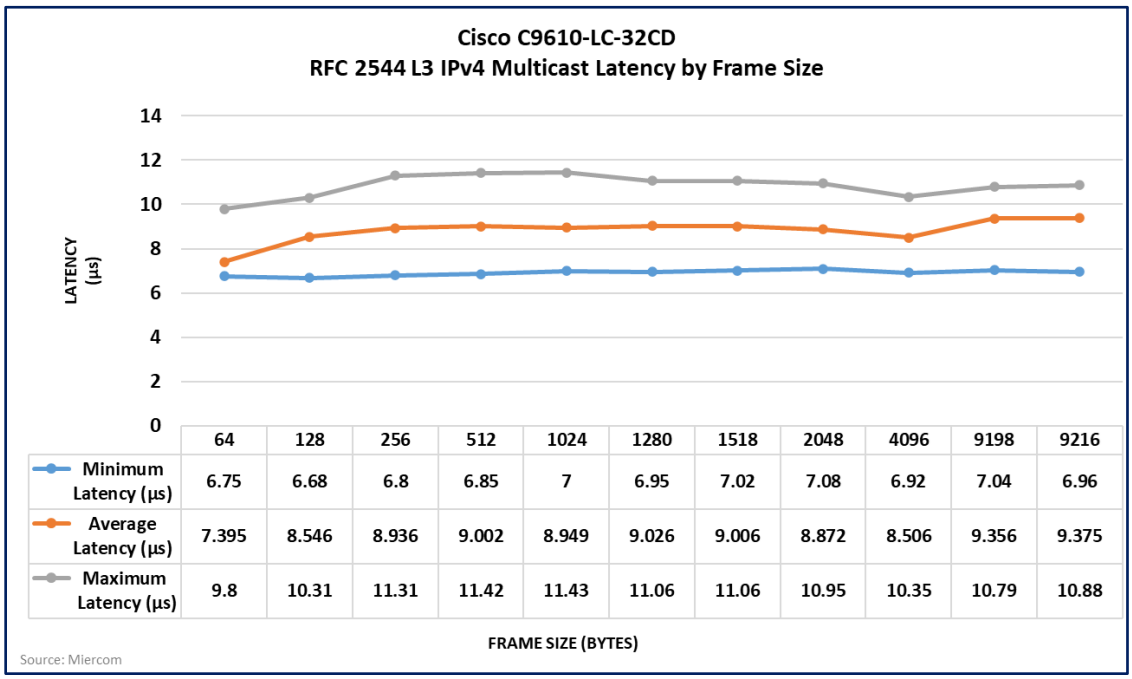
4.2.2 Cisco C9610-LC-32CD L3 IPv4 100G Multicast

The Cisco C9610-LC-32CD delivered full line-rate performance with all 100G ports fully loaded. Throughput reached 100% for all frame sizes with a slight reduction at 64-byte frames. Latency remained stable and low across all frame sizes, with maximum values staying below 11.5 µs.



The Cisco C9610-LC-32CD delivered near-perfect line-rate forwarding. Throughput reached 100% of line rate at all frame sizes from 128 to 9216 bytes, with only a slight reduction at 64-byte frames and no observed frame loss.



	64	128	256	512	1024	1280	1518	2048	4096	9198	9216
Minimum Latency (µs)	6.75	6.68	6.8	6.85	7	6.95	7.02	7.08	6.92	7.04	6.96
Average Latency (µs)	7.395	8.546	8.936	9.002	8.949	9.026	9.006	8.872	8.506	9.356	9.375
Maximum Latency (µs)	9.8	10.31	11.31	11.42	11.43	11.06	11.06	10.95	10.35	10.79	10.88

Latency remained consistently low across all tested frame sizes. Minimum latency stayed around 6.7 to 7.1 µs, average latency ranged from 7.4 to 9.4 µs, and maximum latency remained below 11.5 µs.

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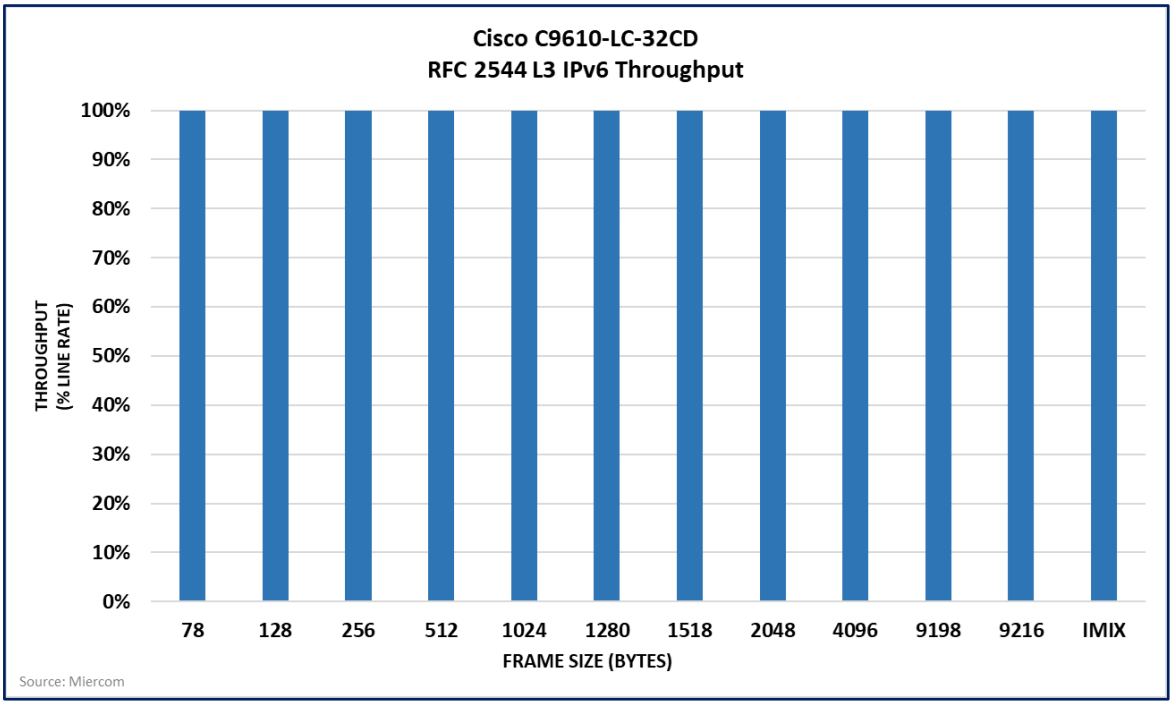
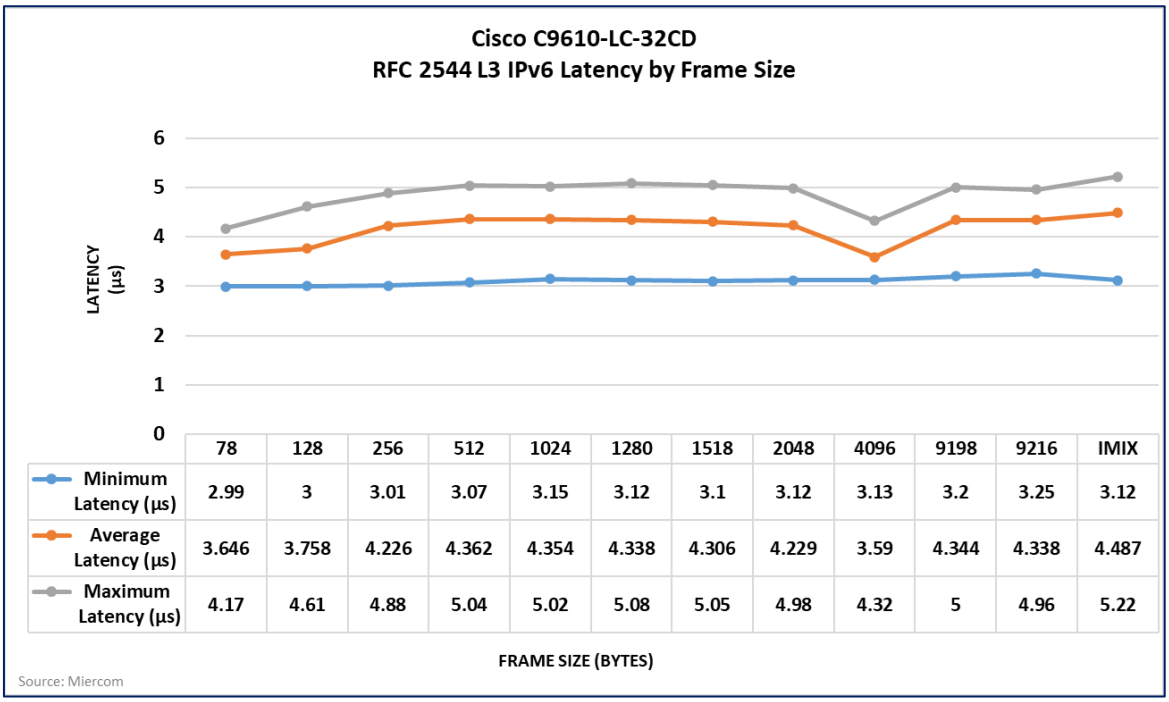
4.2.3 Cisco C9610-LC-32CD L3 IPv6 100G Unicast

The Cisco C9610-LC-32CD delivered full line-rate performance for all frame sizes with all 100G ports loaded. Frame loss was zero throughout.



The Cisco C9610-LC-32CD sustained full line-rate across all frame sizes with all test ports active. Aggregate throughput remained at 100% with zero frame loss from 78 to 9216 bytes and IMIX.



	78	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	2.99	3	3.01	3.07	3.15	3.12	3.1	3.12	3.13	3.2	3.25	3.12
Average Latency (µs)	3.646	3.758	4.226	4.362	4.354	4.338	4.306	4.229	3.59	4.344	4.338	4.487
Maximum Latency (µs)	4.17	4.61	4.88	5.04	5.02	5.08	5.05	4.98	4.32	5	4.96	5.22

The Cisco C9610-LC-32CD maintained lossless, line-rate across all frame sizes and IMIX during testing. Latency stayed in the low-microsecond range across fixed sizes with a small dip in average near 4096 bytes.

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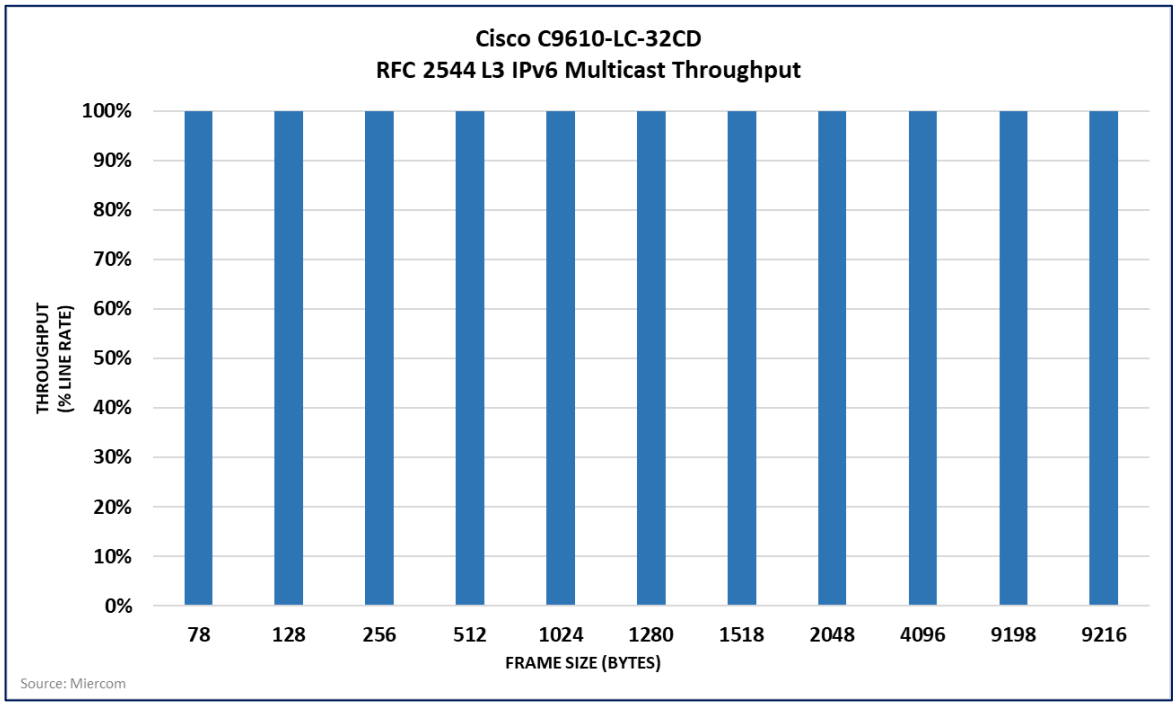
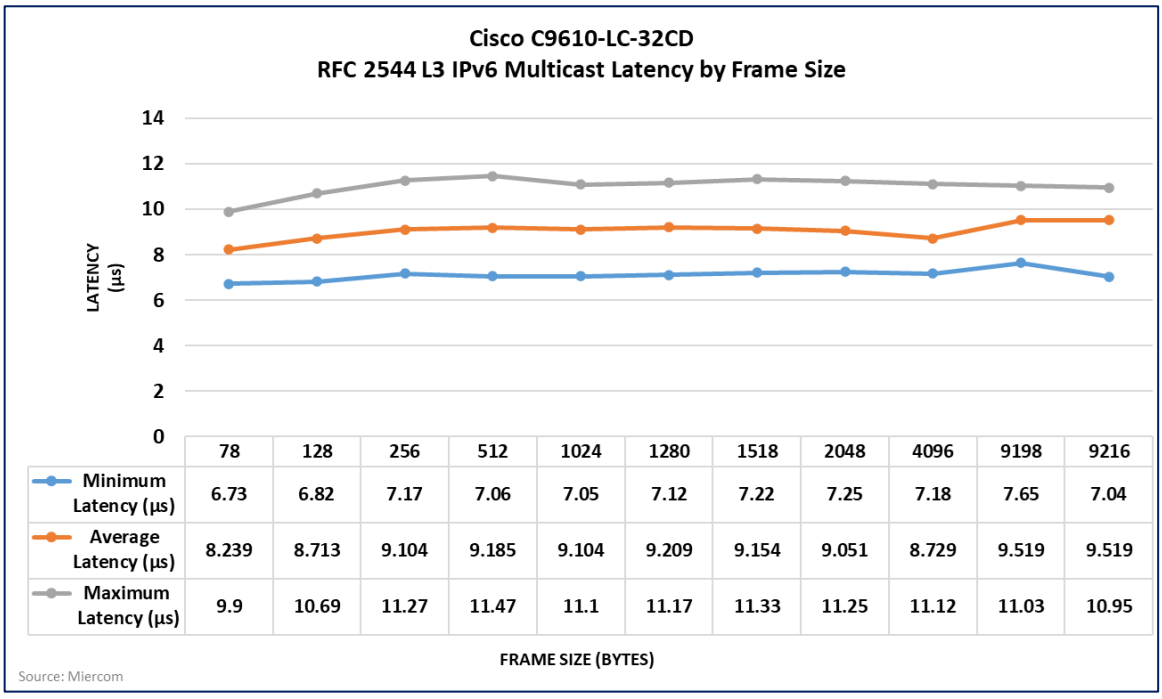
4.2.4 Cisco C9610-LC-32CD L3 IPv6 100G Multicast

The Cisco C9610-LC-32CD delivered full line-rate IPv6 multicast performance with all 100G ports fully loaded. Throughput remained at 100% across all tested frame sizes from 78 to 9216 bytes, with zero frame loss observed. Latency remained stable in the low-microsecond range.



The Cisco C9610-LC-32CD sustained full line-rate forwarding across all frame sizes, with all 100G ports fully loaded and zero frame loss. Throughput remained at 100 percent of line rate for every tested packet size.



Latency was consistent across the full frame-size range. Minimum latency stayed near 6.7 to 7.3 µs, average latency ranged from approximately 8.2 to 9.5 µs, and maximum latency remained below 11.5 µs.

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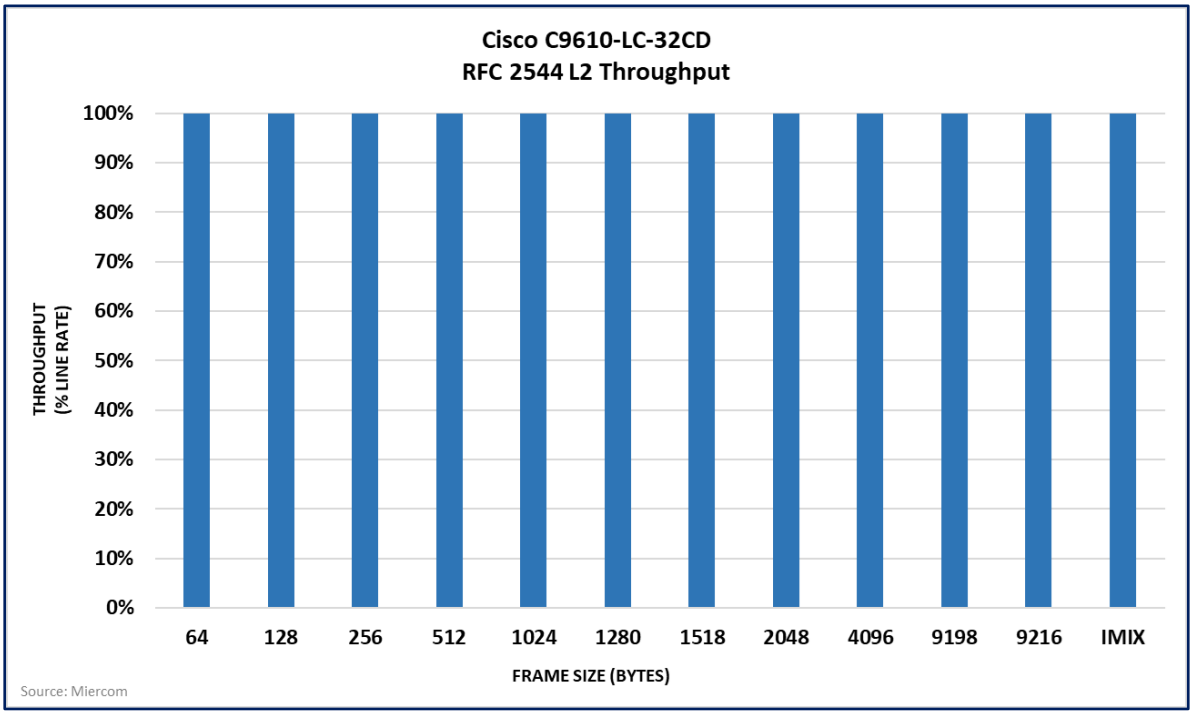
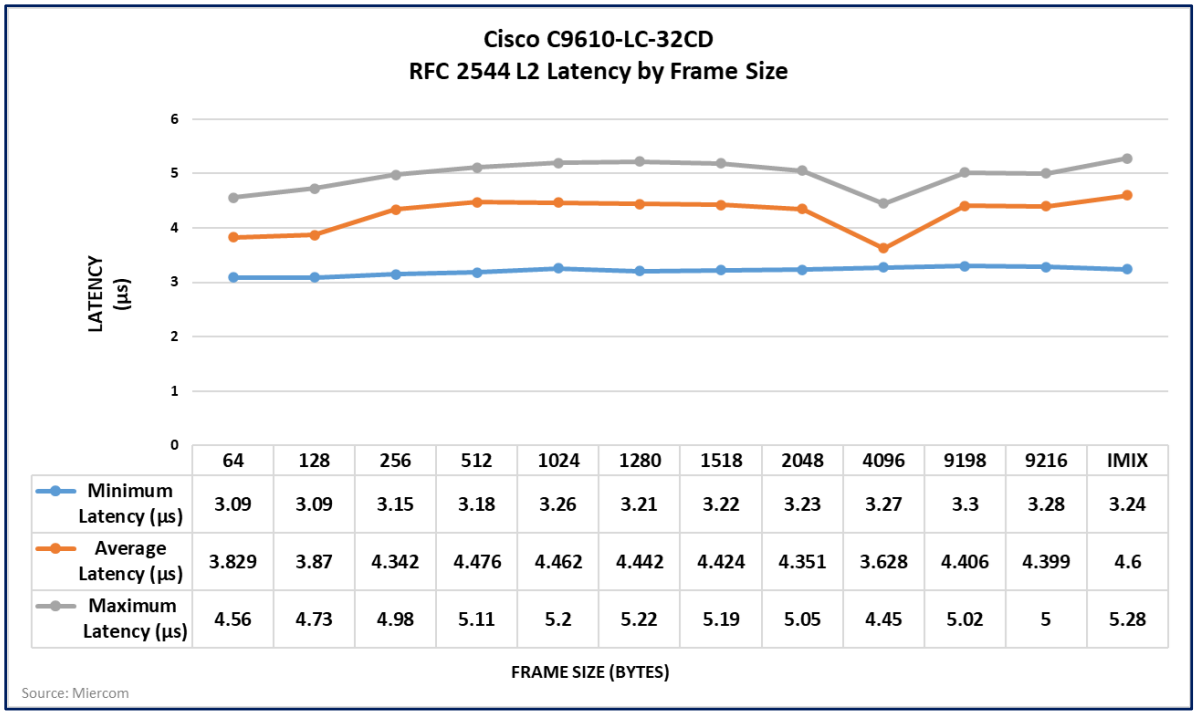
4.2.5 Cisco C9610-LC-32CD L2 100G

The Cisco C9610-LC-32CD delivered full line-rate performance for all frame sizes with all 100G ports loaded. Frame loss was zero throughout.



The Cisco C9610-LC-32CD sustained full line-rate forwarding across all frame sizes with all test ports active. Throughput remained at 100% with zero frame loss from 64 to 9216 bytes; IMIX also achieved 100% with no loss.



	64	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	3.09	3.09	3.15	3.18	3.26	3.21	3.22	3.23	3.27	3.3	3.28	3.24
Average Latency (µs)	3.829	3.87	4.342	4.476	4.462	4.442	4.424	4.351	3.628	4.406	4.399	4.6
Maximum Latency (µs)	4.56	4.73	4.98	5.11	5.2	5.22	5.19	5.05	4.45	5.02	5	5.28

The Cisco C9610-LC-32CD maintained lossless, line-rate forwarding across all frame sizes during RFC 2544 L2 testing. Latency stayed in the low-microsecond range across fixed sizes with a small dip in average near 4096 bytes.

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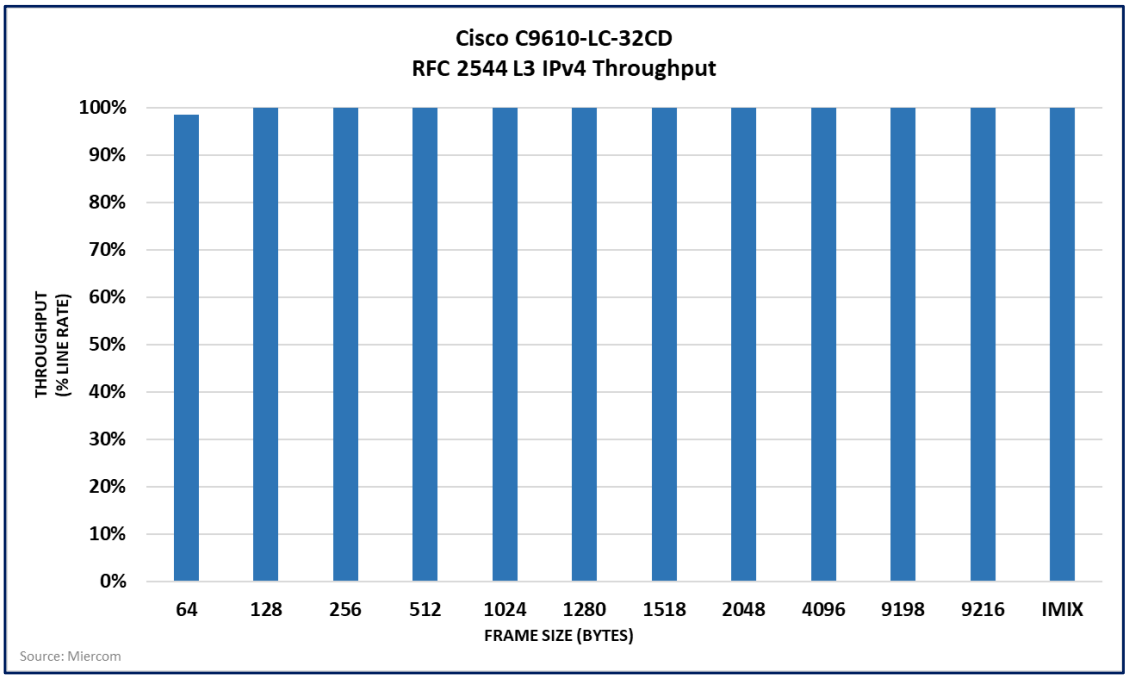
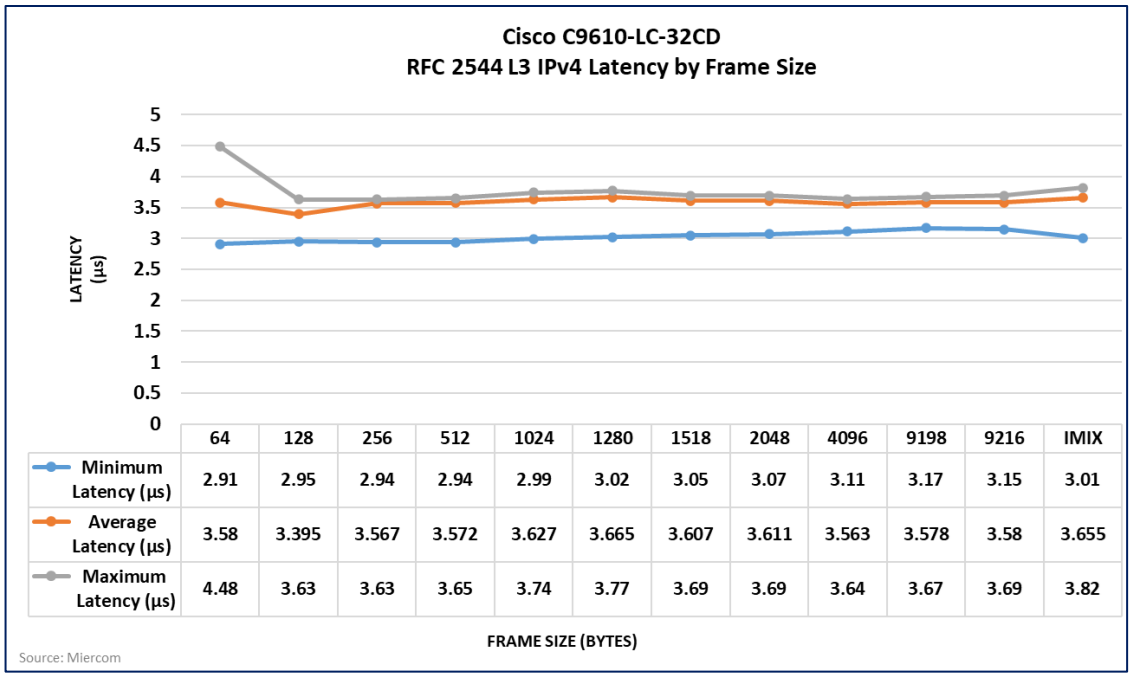
4.2.6 Cisco C9610-LC-32CD L3 IPv4 400G

The Cisco C9610-LC-32CD delivered line-rate IPv4 performance with fully loaded 400G ports. Throughput reached 100 percent of line rate for tested frame sizes from 64 to 9216 bytes and IMIX, with a minor reduction only at 64-byte frames and zero frame loss observed throughout testing.



The Cisco C9610-LC-32CD sustained full line-rate IPv4 forwarding under testing with all 400G ports fully loaded. Throughput remained at 100% of line rate across all fixed frame sizes from 128 to 9216 bytes as well as IMIX traffic, with only a slight reduction observed at 64-byte frames and no frame loss recorded.



	64	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	2.91	2.95	2.94	2.94	2.99	3.02	3.05	3.07	3.11	3.17	3.15	3.01
Average Latency (µs)	3.58	3.395	3.567	3.572	3.627	3.665	3.607	3.611	3.563	3.578	3.58	3.655
Maximum Latency (µs)	4.48	3.63	3.63	3.65	3.74	3.77	3.69	3.69	3.64	3.67	3.69	3.82

Latency was consistently low and stable across all frame sizes and IMIX. Minimum latency stayed near 2.9 to 3.2 µs, average latency ranged from 3.4 to 3.7 µs, and maximum latency remained below 4.5 µs.

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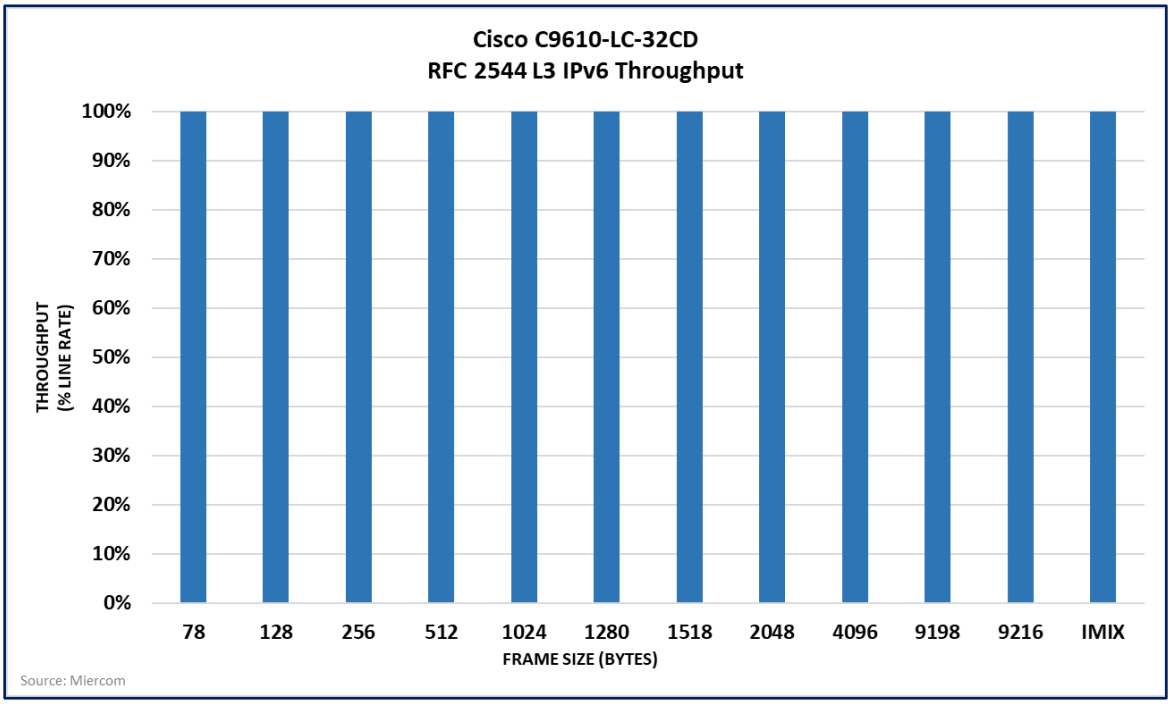
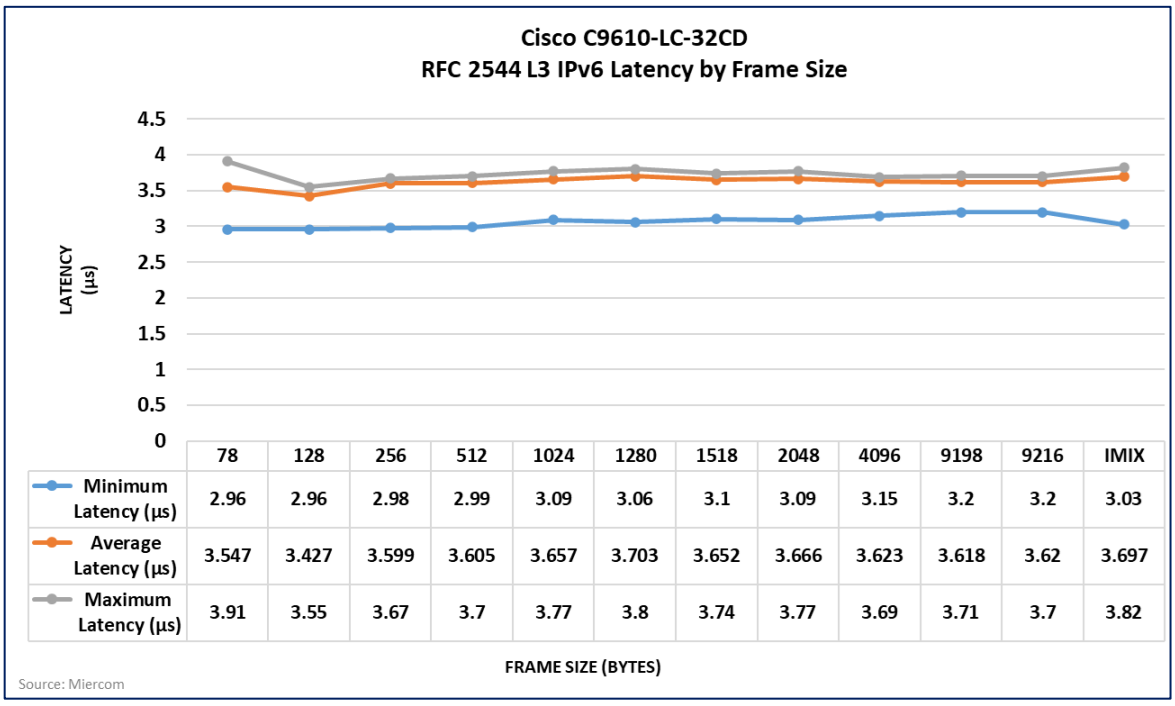
4.2.7 Cisco C9610-LC-32CD L3 IPv6 400G

The Cisco C9610-LC-32CD delivered sustained line-rate IPv6 performance with all 400G ports fully loaded. Throughput remained at 100 percent across all tested frame sizes and IMIX, with zero frame loss and consistently low, stable latency throughout testing.



The Cisco C9610-LC-32CD sustained full line-rate forwarding with fully loaded 400G ports. Throughput remained at 100% of line rate across all tested frames including IMIX traffic, with no frame loss observed.



	78	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	2.96	2.96	2.98	2.99	3.09	3.06	3.1	3.09	3.15	3.2	3.2	3.03
Average Latency (µs)	3.547	3.427	3.599	3.605	3.657	3.703	3.652	3.666	3.623	3.618	3.62	3.697
Maximum Latency (µs)	3.91	3.55	3.67	3.7	3.77	3.8	3.74	3.77	3.69	3.71	3.7	3.82

Latency performance remained consistent across all frame sizes and IMIX. Minimum latency stayed near 3.0 µs, average latency ranged from approximately 3.4 to 3.7 µs, and maximum latency remained below 3.9 µs.

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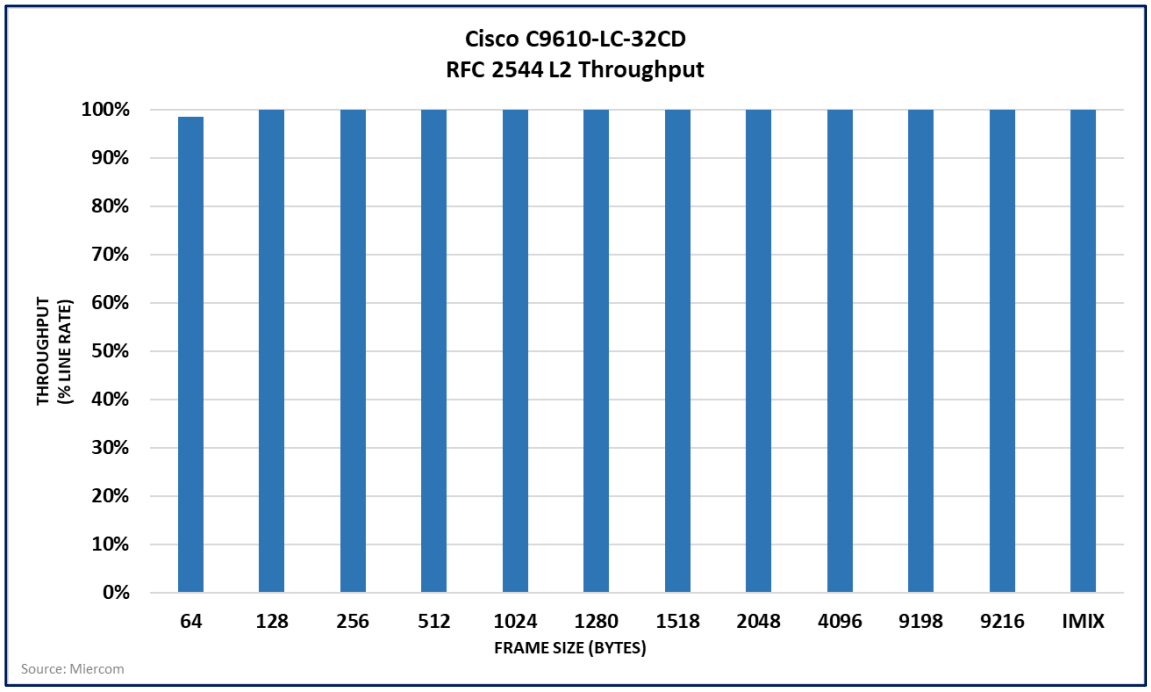
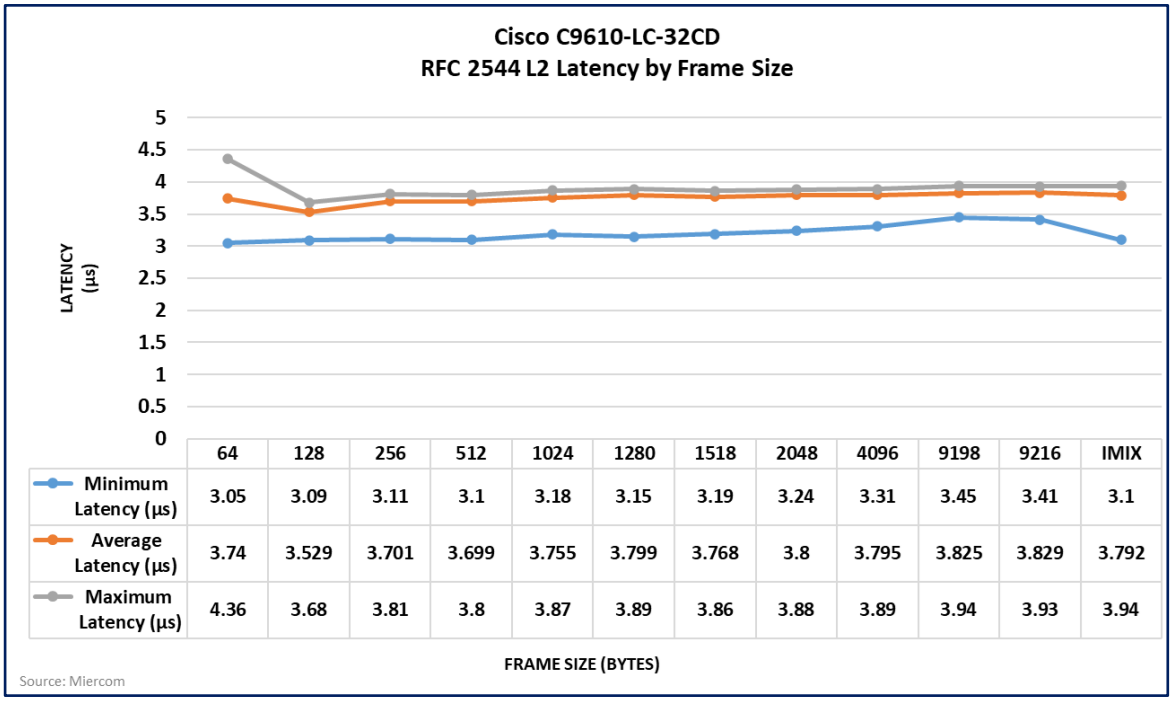
4.2.8 Cisco C9610-LC-32CD L2 400G

The Cisco C9610-LC-32CD delivered sustained line-rate Layer 2 performance with all 400G ports fully loaded. Throughput reached 100 percent of line rate across all tested frame sizes and IMIX traffic, with zero frame loss and consistently low, predictable latency throughout testing.



The Cisco C9610-LC-32CD sustained line-rate Layer 2 forwarding with all 400G ports fully loaded. Throughput remained at 100 percent of line rate across all fixed frame sizes from 128 to 9216 bytes as well as IMIX traffic, with only a slight reduction observed at 64-byte frames and no frame loss recorded.



	64	128	256	512	1024	1280	1518	2048	4096	9198	9216	IMIX
Minimum Latency (µs)	3.05	3.09	3.11	3.1	3.18	3.15	3.19	3.24	3.31	3.45	3.41	3.1
Average Latency (µs)	3.74	3.529	3.701	3.699	3.755	3.799	3.768	3.8	3.795	3.825	3.829	3.792
Maximum Latency (µs)	4.36	3.68	3.81	3.8	3.87	3.89	3.86	3.88	3.89	3.94	3.93	3.94

Layer 2 latency remained stable across all frame sizes and IMIX. Minimum latency ranged from approximately 3.0 to 3.5 µs, average latency stayed between about 3.5 and 3.8 µs, and max latency remained below 4.4 µs.

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4.3 Cisco C9610-SUP-3XL FIB Scale with Default SDM Template

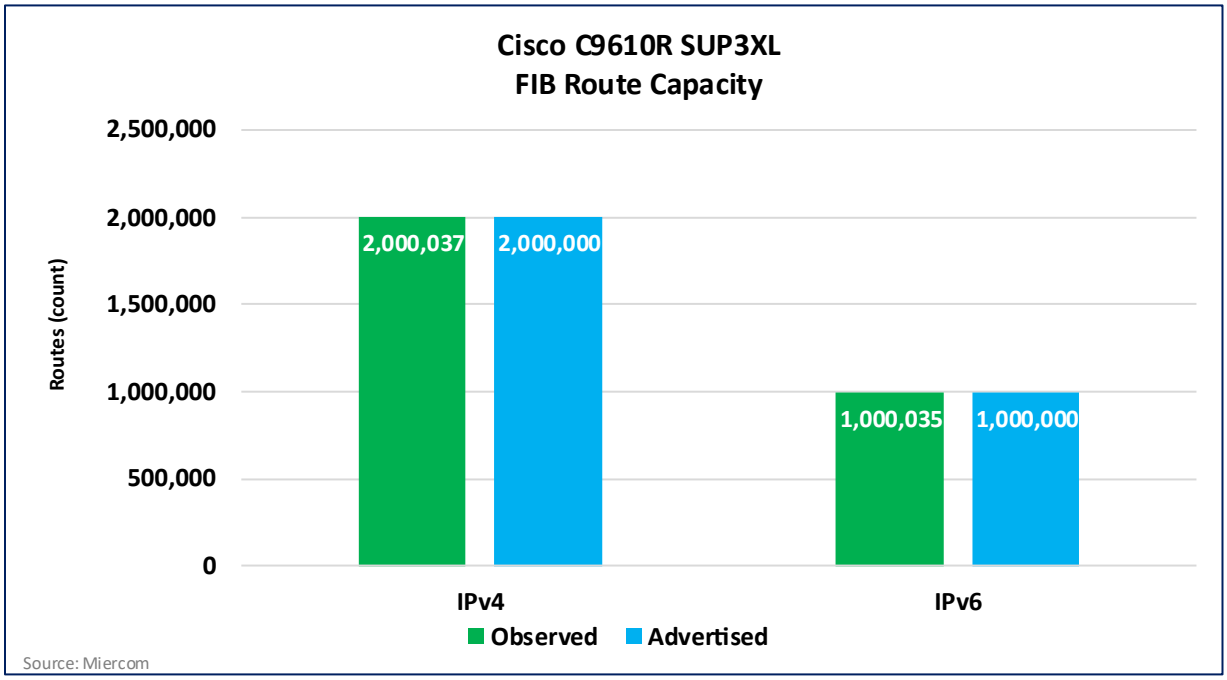
This section focuses on the Forwarding Information Base (FIB) capacity and stability validation. Routing entries change frequently in production networks; in high-capacity cores, those changes must not introduce delay or loss. A core switch is expected to carry large routing tables while maintaining performance and scale.

The Cisco C9610R Smart Switches with Supervisor 3XL has a default routing-optimized SDM/TCAM profile that partitions resources for Layer-3 scaling (target 2M IPv4 / 1M IPv6 LPM entries).

Using Spirent TestCenter, we measured the maximum hardware-installed routes the device could sustain while forwarding traffic to every advertised prefix via eBGP.

The device was set to a maximum of 2,000,000 IPv4 and 1,000,000 IPv6 routes. We observed 2,000,037 IPv4 and 1,000,035 IPv6 routes installed in hardware—effectively ~100% of the stated capacities (a +37 and +35 route margin, respectively).

C9610R	Target (routes)	Observed (routes)	% of Target	Delta
IPv4	2,000,000	2,000,0037	100%	+37
IPv6	1,000,000	1,000,0035	100%	+35



Cisco C9610-Sup-3XL FIB routes exceeded the advertised scale. The switch programmed 2,000,037 IPv4 vs 2,000,000 advertised and 1,000,035 IPv6 vs 1,000,000 advertised. A small overage that shows Cisco's conservative, supported limits and provides operational margin for the route churn and feature overhead while maintaining

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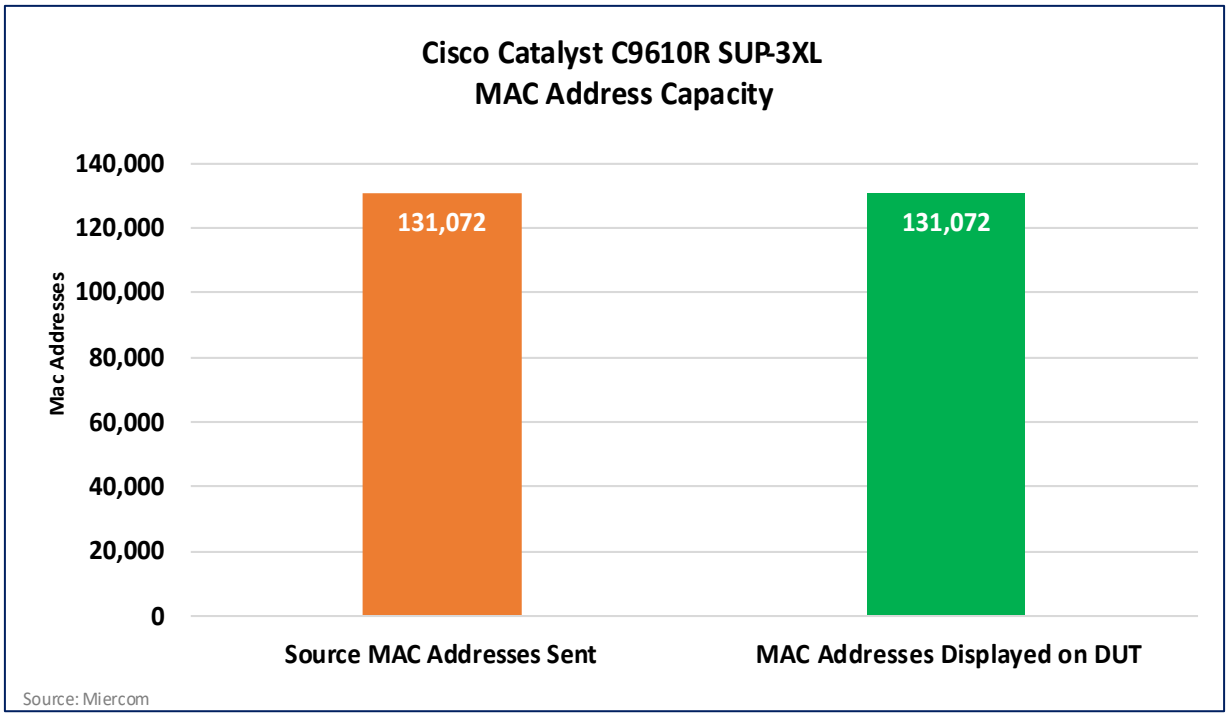
4.4 Cisco C9610-SUP-3XL MAC Scale with Default SDM Template

This test validates MAC address table capacity and learning behavior. Using Spirent TestCenter RFC 2889 Address Caching Capacity, we injected a controlled stream of unique source MAC addresses and verified the learned count and population time on the DUT.

The C9610R equipped with Supervisor 3XL and C9610-LC-32CD, Spirent was configured for 64-byte frames, 1,000 frames/sec learning rate, and 300-second aging, with a target of 131,072 unique MAC addresses. The switch reported 131,072 dynamic MAC addresses in use with 0 remaining address space, confirming the configured scale was achieved. The observed population time was ≈ 2:07.



Using Spirent TestCenter RFC 2889 Address Caching Capacity with 64-byte frames and a learning rate of 1,000 frames/sec, the DUT learned and reported 131,072 unique source MAC addresses, matching the number sent. Device counters show mac address-table count = 131,072 dynamic entries with 0 address space remaining, and platform output confirms MAC FORWARDING TABLE = 131,072 entries. Approximate learning duration: ~2 min 07 sec.

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4.5 Cisco C9610R High Availability

The Cisco C9610R supports high availability through a dual-supervisor architecture, providing Stateful Switchover (SSO) with Non-Stop Forwarding (NSF) and In-Service Software Upgrade (ISSU) capabilities. These mechanisms are designed to maintain control-plane continuity and preserve data-plane forwarding during supervisor failures and software upgrades.

High availability testing was performed on a single C9610R chassis populated with dual Supervisor 3XL modules and C9610-LC-32CD line cards. Both supervisors were running the same Cisco IOS XE software release and were configured in SSO mode.

4.5.1 Stateful Switchover (SSO) and Non-Stop Forwarding (NSF)

SSO maintains a hot-standby supervisor that synchronizes control-plane state with the active supervisor. In the event of a supervisor failure or forced switchover, the standby supervisor assumes the active role without requiring a full system reload. NSF allows the forwarding plane to continue passing traffic during the control-plane transition by relying on neighboring devices to preserve forwarding state.

During testing, the C9610R operated with one Supervisor 3XL module in the active role and one in standby, both confirmed to be operating in SSO mode. Module and redundancy status outputs verified proper supervisor role assignment and synchronization.

```
C9610-P2B-TME#sh module
Chassis Type: C9610R

Mod Ports Card Type                                  Model          Serial No.
---+-----+--------------------------------------+-------------+-------------
1   32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD026270DFP
2   32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD026270G39
3   32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD0261800XC
4   32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD026030AA8
5   0    Supervisor 3XL Module                     C9610-SUP-3XL    FD0292900BJ
6   0    Supervisor 3XL Module                     C9610-SUP-3XL    FD029290033
7   32   30x40/100GE + 2x40/100/400GE              C9610-LC-32CD    FD0291607TU
8   32   30x40/100GE + 2x40/100/400GE              C9610-LC-32CD    FD0291607U1
9   32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD0261800X0
10  32   30x40/100GE + 2x40/100/400GE              C9600X-LC-32CD   FD026270G33

Mod Redundancy Role     Operating Redundancy Mode Configured Redundancy Mode
---+------------------+-------------------------+---------------------------
5   Active              sso                       sso
6   Standby             sso                       sso
```

Supervisor redundancy state showing active and standby Supervisor 3XL modules operating in SSO mode.

Traffic was generated across multiple 100G interfaces while a supervisor switchover event was initiated. Forwarding continuity was maintained during the transition, and no full data-plane outage was observed. The standby supervisor successfully assumed the active role, and traffic forwarding resumed normal operation immediately following the switchover.

Observation

- Active and standby supervisors remained synchronized prior to switchover.
- Forwarding continued during the supervisor role transition.
- No line card reloads were observed.
- No manual intervention was required to restore forwarding.

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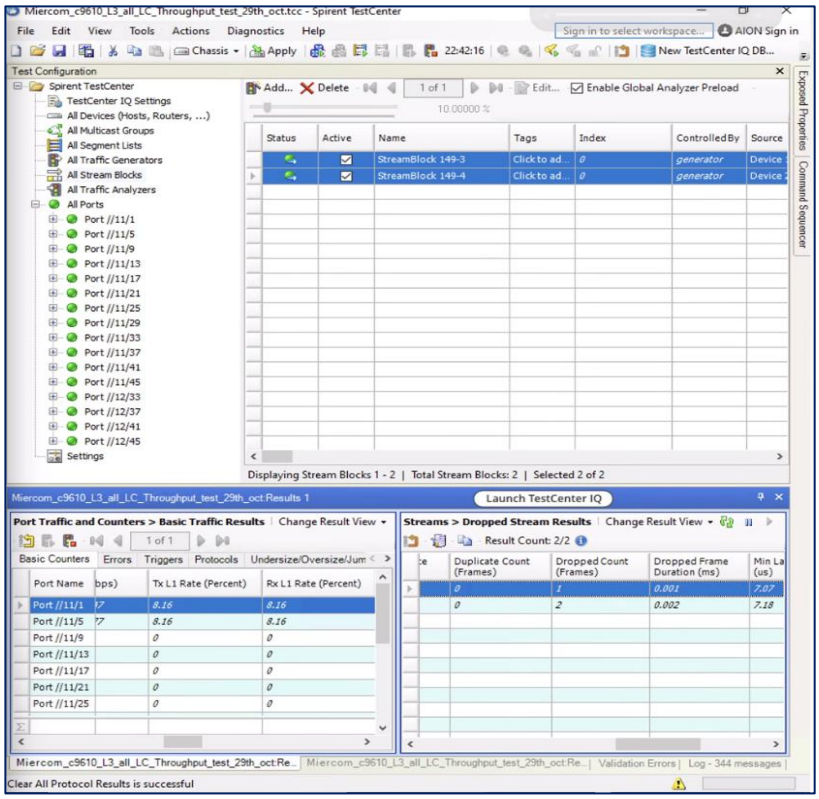
4.5.2 In-Service Software Upgrade (ISSU)

ISSU enables software upgrades on the Cisco C9610R while maintaining traffic forwarding by leveraging the SSO/NSF architecture. The ISSU workflow upgrades the standby supervisor first, performs an automatic supervisor switchover, and then upgrades the former active supervisor before completing the operation.

ISSU capability requires both supervisors operating in install mode and configured for SSO. The system reported no ISSU operation in progress before execution.

The ISSU process was executed using the standard install add, install activate issu, and install commit workflow. During the upgrade, the standby supervisor was reloaded with the new software image, followed by an automatic supervisor switchover. The former active supervisor was then upgraded and returned to standby before the operation was committed.

Traffic generation remained active throughout the ISSU process. Brief, sub-second traffic convergence events were observed during supervisor reload and role transition phases. No sustained traffic loss was observed and forwarding resumed normal operation after each transition.



Traffic generation stayed active during the ISSU process with brief convergence observed during supervisor reload and role transition events.

Observation

- ISSU prerequisites were met and verified prior to execution.
- Automatic supervisor switchover occurred as expected.
- Traffic forwarding was maintained with brief (subseconds) convergence during supervisor reloads.
- ISSU completed successfully and was committed without rollback.
- Post-upgrade status confirmed both supervisors running target software version in SSO mode.

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4.6 Cisco C9610R Solutions

4.6.1 Post-Quantum Cryptography (PQC)

Post-Quantum Cryptography (PQC) on Cisco C9000 Series Smart Switches platforms strengthens the device trust chain and transport protocols with NIST-approved PQC algorithms.

Secure Boot

Secure Boot ensures that every Cisco C9000 Smart Switch powers on with a cryptographically verified, tamper-resistant chain of trust, ensuring that only authenticated and unmodified software is allowed to run. The process begins with a microloader embedded in the FPGA that is encrypted and authenticated using AES-GCM-256. This microloader validates the bootloader, which is signed using LMS (Leighton–Micali Signature), a NIST-approved post-quantum cryptography (PQC) algorithm. The bootloader then verifies the IOS-XE image, which is signed with ML-DSA (Module-Lattice-Based Digital Signature Algorithm), another NIST-approved PQC algorithm, completing the secure boot sequence. In addition, ML-KEM (Module-Lattice-Based Key-Encapsulation Mechanism) is used to secure the bus interfaces between the CPU and TAm, preventing the leakage of confidential information across internal interfaces.

Secure Transport

Key exchange mechanisms used by protocols like MACsec, IPsec, TLS and SSH rely on Diffie–Hellman, an asymmetric algorithm expected to be vulnerable to attacks from future quantum computers. To address this risk, ML-KEM (Module-Lattice-Based Key-Encapsulation Mechanism) is being implemented in Cisco C9000 Smart Switches for EAP-TLS 1.3 to support certificate-based MACsec, for IKEv2 in IPsec, and for general use in TLS 1.3 and SSH. As a result, all critical network protocols benefit from quantum-resistant key exchange. Administrators will be able to select ML-KEM when configuring their switches, ensuring that data in transit is protected against quantum threats.

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